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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,324	08/27/2001	Robert T. George	2207/12003	5090
25693	7590	08/11/2005	EXAMINER	
KENYON & KENYON (SAN JOSE) 333 WEST SAN CARLOS ST. SUITE 600 SAN JOSE, CA 95110			KIM, HONG CHONG	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,324	GEORGE ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 20 July 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-17 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

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Detailed Action

1. Claims 1-17 are presented for examination. This office action is in response to the amendment filed on 7/20/05.

Terminal Disclaimer

2. The terminal disclaimer filed on 7/20/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 10/231,414 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 9-15 are rejected under 35 U.S.C. 102(e) s being anticipated by Solomon et al. (Solomon) U.S. Patent No. 6,751,705.

As to claim 9, Solomon discloses the invention as claimed. Solomon discloses a method comprises receiving a transaction request (col. 5 lines 22-30) at one of a plurality of client ports (Fig. 15 Refs. 120 and 220 and Fig. 2 Ref. 1600)) on a I/O

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cache-coherent device (Fig. 2 ref. 26 and col. 6 lines 11-20), said transaction request includes an address (col. 5 lines 22-30 and Fig. 5); and determining whether said address is present (col. 8 lines 1-3, cache hit or miss reads on this limitation) in one of a plurality of sub-unit caches (Fig. 15 refs. 112's), each of said sub-unit caches assigned to said one of said plurality of client ports.

As to claim 10, Solomon discloses the invention as claimed in the above.

Solomon further discloses wherein said transaction request is a read transaction request (col. 5 lines 22-30 and fig. 11 Ref. 82).

As to claim 11, Solomon discloses the invention as claimed in the above.

Solomon further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports (col. 5 lines 22- 30 and Fig. 5).

As to claim 12, Solomon discloses the invention as claimed in the above.

Solomon further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities and col. 5 lines 22-35); and updating the coherency state (col. 4 lines 21-39) information in said plurality of sub-unit caches.

As to claim 13, Solomon discloses the invention as claimed in the above.

Solomon further discloses wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 4 lines 21-39).

As to claim 14, Solomon discloses the invention as claimed in the above.

Solomon further discloses wherein said transaction request is a write transaction request (Fig. 11 Ref. 78).

As to claim 15, Solomon discloses the invention as claimed in the above.

Solomon further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and col. 4 lines 21-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4 . Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al. (Solomon) U.S. Patent No. 6,751,705 in view of Yasuda et al. (Yasuda) U.S. Patent No. 6,636926.

As to claim 1, Solomon discloses a cache-coherent I/O device (Fig. 15) comprising: a plurality of client ports (Fig. 15 Refs. 120 & 220 and Fig. 2 Ref. 22 & 1600), each to be coupled to one of a plurality of port components (Fig. 15 Refs. 118 and 218); and a plurality of sub-unit caches (Fig. 15 Refs. 112's), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components (Fig. 15).

However, Solomon does not specifically disclose a coherency engine coupled to said plurality of sub-unit caches.

Yasuda discloses a coherency engine (Fig. 1 Ref. 330) coupled to said plurality of sub-unit caches for the purpose of maintaining data consistency thereby increasing the memory access speed by preventing cache error.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a coherency engine coupled to said plurality of sub-unit caches of Yasuda into the invention of Solomon for the advantages stated above.

As to claim 2, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said plurality of port components includes processor port components (Fig. 15 Refs. 118 and 218).

As to claim 3, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said plurality of port components includes input/output components (Fig. 15 Ref. 118).

As to claim 4, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said plurality of sub-unit caches includes transaction buffers (Fig. 2 Ref. 26). Yasuda further discloses a coherency logic protocol (Fig. 1 Ref. 330).

As to claim 5, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 4 lines 21-39).

As to claim 6, Solomon discloses a cache-processing system comprising (Fig. 15): a processor (Fig. 15 Ref 118); a plurality of port components (Fig. 15 Refs 120 and 220 each including Fig. 2 Ref. 22); and a cache-coherent I/O device (col. 6 lines 11-20) coupled to said processor and including a plurality of client ports (Fig. 2 Ref. 1600), each coupled to one of said plurality of port components (Fig. 2 Ref. 22), said cache-coherent device further including a plurality of caches (Fig. 15 Refs. 112's), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components.

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However, Solomon does not specifically disclose a coherency engine coupled to said plurality of sub-unit caches.

Yasuda discloses a coherency engine (Fig. 1 Ref. 330) coupled to said plurality of sub-unit caches for the purpose of maintaining data consistency thereby increasing the memory access speed by preventing cache error.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a coherency engine coupled to said plurality of sub-unit caches of Yasuda into the invention of Solomon for the advantages stated above.

As to claim 7, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said plurality of port components includes processor port components (Fig. 15 Refs. 118 and 218).

As to claim 8, Solomon and Yasuda disclose the invention as claimed in the above. Solomon further discloses wherein said plurality of port components includes input/output components (Fig. 15 Refs. 118 and 218).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al. (Solomon) U.S. Patent No. 6,751,705 in view of Witt et al. (Witt) U.S. Patent 6,202,139.

As to claim 16, Solomon further discloses modifying coherency state information of said write transaction request (col. 5 lines 21-30 and Fig. 11 Ref. 78), however, Solomon does not specifically discloses write transaction request in the order received and pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining multiple write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts thereby decreasing the performance losses and increasing the access speed (col. 2 lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate write transaction request in the order received and pipelining multiple write requests as shown in Witt into the invention of Solomon because it would avoid bank conflicts thereby decreasing the performance losses and increasing the access speed.

As to claim 17, Solomon and Witt disclose the invention as claimed in the above. Solomon further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 5 lines 21-38).

Response to Arguments

6. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

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H Kim
Primary Patent Examiner
August 7, 2005

A handwritten signature in black ink, appearing to read "H Kim".